Amendments to the Specification

On page 2,in the brief description of the drawings section please add the following new paragraphs at the end of that section:

Figure 2e is a time plot showing a step function.

Figure 2f is a time plot showing trigger pulses.

On page 4, for the paragraph starting at line 6:

The V-sync pulses are processed in the trigger logic unit 30 into the trigger signal 130 as shown in Figures 2a to 2f. As mentioned above, there are two V-sync pulses, associated with two interlaced fields, for every image frame. Thus, only one of the two is used for triggering the light source 20. The two interlaced fields for each frame are herein referred to as odd and even fields, and the two associated V-sync pulses are referred to as odd (O) and even (E) sync pulses, as shown in Figure 2a. Advantageously, the V-sync pulses are shaped by a pulse shaping circuit, such as a comparator, into a series of rectangular pulses, as shown in Figure 2b. Through a divided-by-two circuit, such as a flip-flop, the rectangular pulses are converted into a series of square pulses, as shown in Figure 2c. With an edge triggering circuit, such as a monostable logic chip, the square-pulses are converted into a series of short pulses, each for an image frame, as shown in Figure 2d. Preferably, the light source 20 is triggered to produce flashes only when the mail-related item 200 is present in the field-of-view of the camcorder 10. Thus, the output 110 of the sensor 32 is processed by the trigger logic unit 30 into a step-like function, as shown in Figure ~~3e~~2e, to enable an AND-gate, for example, to admit the trigger pulses only when the mail-related item 200 is present in the field-of-view of the camcorder 10, as shown in Figure ~~3f~~2f. Each of these trigger pulses is denoted as the trigger signal 130 in Figure 1.